SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

93C06/46 -I /P

Package:		J	CERDIP
		P	Plastic DIP
		SN	Plastic SOIC (150 mil Body)
		SM	Plastic SOIC (207 mil Body)
Temperature Range:		Blank	0°C to +70°C
		I	-40°C to +85°C
		E	-40°C to +125°C
Device:		93C06	256 bit CMOS Serial EEPROM
		93C46	1K CMOS Serial EEPROM
		93C46X	1K CMOS Serial EEPROM with alternate pinouts (in SN package only)
		93C06T	(in Tape and Reel)
		93C06/46T	(in Tape and Reel)
		93C46XT	(in Tape and Reel)

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MICROCHIP

93C56/66

2K/4K 5V CMOS Serial EEPROM

FEATURES

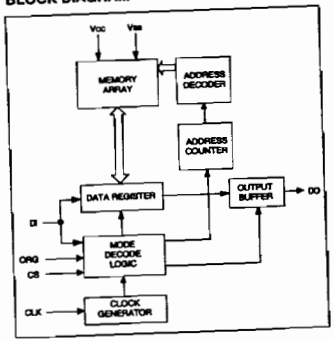
- Low power CMOS technology
- ORG pin selectable memory organization
  - — 256 x 8 or 128 x 16 bit organization (93C56)
  - — 512 x 8 or 256 x 16 bit organization (93C66)
- Single 5 volts only operation
- Max clock at 2 MHz
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8-pin PDIP/SOIC packages (SOIC in JEDEC and EIAJ standards)
- Available for extended temperature ranges:
  - — Commercial: 0°C to + 70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C
- 1 ms byte write time

DESCRIPTION

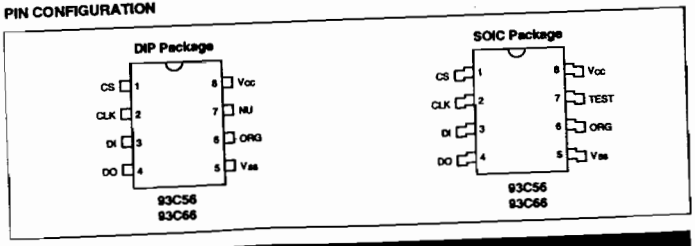
The Microchip Technology Inc. 93C56/66 family of Serial EEPROMs are configurable to either x16 or x8 organization. The ORG pin is used to select the desired configuration. Advanced CMOS technology makes this device ideal for low-power non-volatile memory applications. The 93C56/66 are available in the standard 8-pin DIP and 8-pin surface mount SOIC package.

This device offers fast (1 ms) byte write and extended (-40°C to 125°C) temperature operation. It is recommended that all other applications use Microchip's 93LC56/93LC66.

BLOCK DIAGRAM



PIN CONFIGURATION



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ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) . +300°C
ESD protection on all pins ..... 3 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
ORG	Memory Array Organization
Test	Connect to Vss or Vcc
Vcc	Power Supply +5V

DC AND AC ELECTRICAL CHARACTERISTICS

Commercial (C): Tamb = 0°C to +70°C Vcc = +5V (±10%)
Industrial (I): Tamb = -40°C to +85°C Vcc = +5V (±10%)
(Note 2) Automotive (E): Tamb = -40°C to +125°C Vcc = +5V (±10%)

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.3	4.5	V	
High level input voltage	VIH	2.0	Vcc + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA
Input leakage current	ILI	—	10	µA	VIN = 0V to Vcc
Output leakage current	ILO	—	10	µA	VOUT = 0V to Vcc
Output capacitance	COUT	—	7	pF	VIN/VOUT = 0V; Note 1
Input capacitance	CIN	—	7	pF	VIN/VOUT = 0V; Note 1
Operating current (all modes)	ICC write	—	4	mA	FCLK = 2 MHz; Vcc = 5.5V
Standby current	ICCS	—	130	µA	CS = 0V; Vcc = 5.5V; x 6 org
	—	—	100	µA	CS = 0V; Vcc = 5.5V; x 16 org
Endurance	—	100,000	—	E/W Cycles	
Clock frequency	FCLK		2	MHz	
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	100	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF
Status valid time	TSV	—	100	ns	CL = 100 pF
Program cycle time (auto ERASE and WRITE)	TWC	—	1	ms	(x 8 organization)
		—	2	ms	(x 16 organization)
	TEC	—	15	ms	ERAL & WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz. It is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

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INSTRUCTION SET FOR 93C56

ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/BSY)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	12
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	20
WRAL	1	00	0 1 X X X X X X	D7 - D0	(RDY/BSY)	20
EWDS	1	00	0 0 X X X X X X	—	High-Z	12

INSTRUCTION SET FOR 93C66

ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/BSY)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X	—	High-Z	12
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	12
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	12
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	20
WRAL	1	00	0 1 X X X X X X	D7 - D0	(RDY/BSY)	20
EWDS	1	00	0 0 X X X X X X	—	High-Z	12

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FUNCTIONAL DESCRIPTION

The 93C56/66 family can be organized x16 or x8. When the ORG pin is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the (x16) organization. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CLK.

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all modes of operation are inhibited until Vcc has reached 2.3 V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below 2.3 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

ERASE/WRITE ENABLE AND DISABLE

The 93C56/66 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data changes, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 1 ms per byte maximum.

WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

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The DO pin indicates the READY/BUSY status of the device if CS is brought high after a minimum of 100 ns (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 1 ms per byte maximum.

ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1". The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL).

The ERAL cycle takes 15 ms maximum.

WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does not include an automatic ERASE cycle for the device. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL).

The WRAL cycle takes 15 ms maximum.

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C56/66. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/BUSY status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) and an ERASE or WRITE operation has been initiated.

Organization (ORG)

When ORG is connected to Vcc, the (x16) memory organization is selected. When ORG is tied to Vss, the (x8) memory organization is selected. When ORG is left floating, an internal pullup device will select the device in (x16) organization.

Test

This pin is used for test mode only. It is recommended to connect to Vcc or Vss for normal operation.

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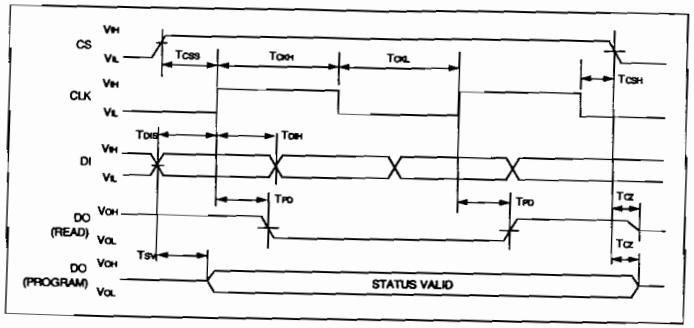
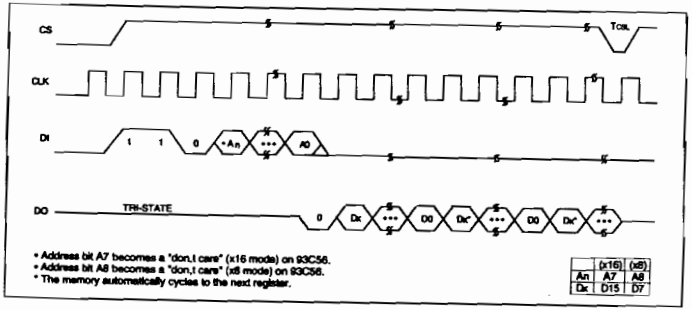
TIMING DIAGRAMS

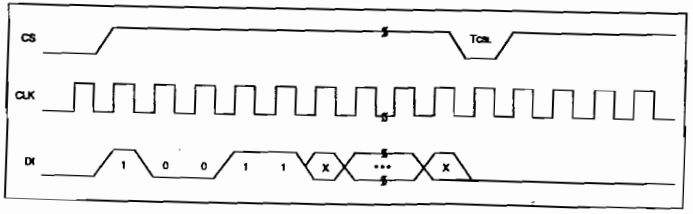
SYNCHRONOUS DATA TIMING



READ



EWEN



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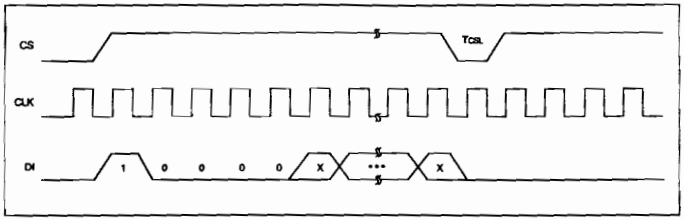
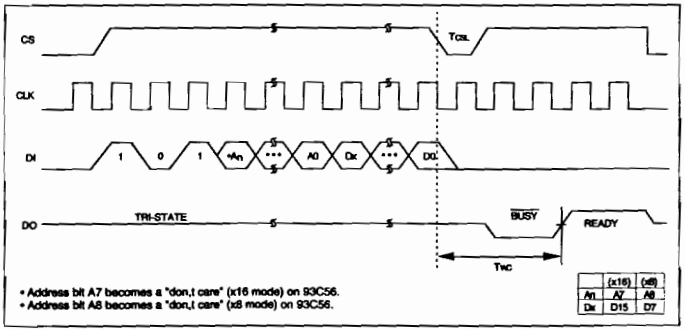
TIMING DIAGRAMS (Cont.)

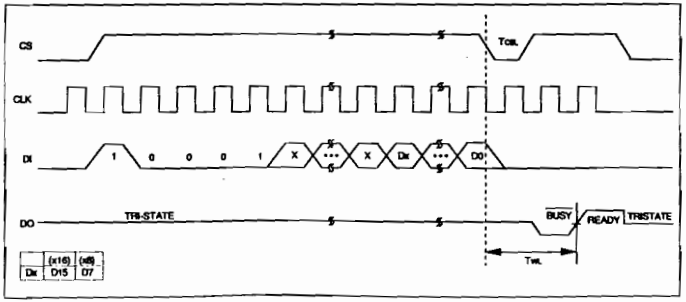
EWDS



WRITE



WRAL



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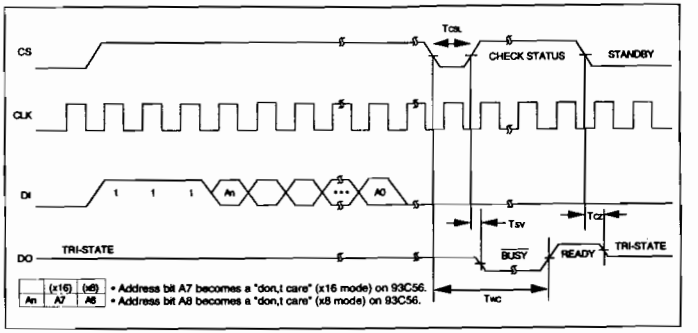
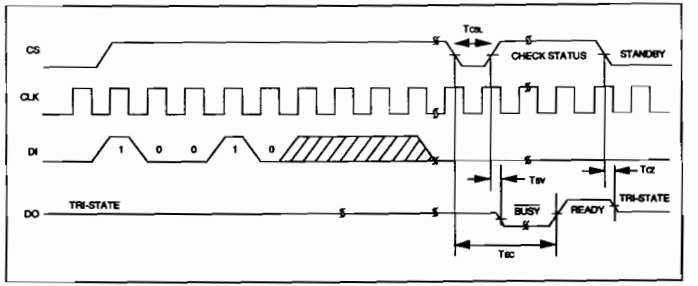
TIMING DIAGRAMS (Cont.)

ERASE



ERAL



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NOTES

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